

SPECIFICATION FOR TFT MODULE

MODULE No.:TFT035A101C

CUSTOMER APPROVAL:

	SIGNATURE	DATE
PREPARED BY	为和类	2018-03-02
CHECKED BY	\$ Z	2018-03-02
APPROVED BY		2018-03-02

Notes:

- 1. Please contact GTK before assigning your product based on this module specification.
- 2. To improve the quality of product, and this product specification is subject to change without any notice.

REVISION RECORD

Rev No.	Rev date	Contents	Remarks
0	2018-03-02	First release	Preliminary

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1. GENERAL INFORMATION

No.	Item	Contents	Unit
1	LCD size	3.5 inch (Diagonal)	/
2	LCD type	TN/Normally white/Transmissive	1
3	Viewing direction(eye)	6 O'clock	1
4	Gray scale inversion direction	12 O'clock	1
5	Resolution(H*V)	320 *480 Pixels	1
6	Module size (L*W*H)	55.50*84.96*5.43	mm
7	Active area (L*W)	48.96*73.44	mm
8	Pixel pitch (L*W)	0.153*0.153	mm
9	Interface type	MCU interface /RGB interface	/
10	Module power consumption	TBD	W
11	Back light type	LED	/
12	Driver IC	ILI9488 or compatible	/
13	Weight	TBD	g

2. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min.	Max.	Unit
Power supply input voltage(TFT Module)	VDD	-0.3	4.6	V
Backlight current (normal temp.)	ILED	-	75	mA
Operation temperature	Тор	-20	+70	°C
Storage temperature	Tst	-30	+80	°C
Humidity	RH	-	90%(Max60 °C)	RH

3. ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS(at Ta=25°C)

Item	Symbol	Min.	Тур.	Max.	Unit	Note
Power supply input voltage(TFT Module)	VDD	2.5	2.8	3.3	V	
I/O logic voltage	VDDIO	1.65	1.8	3.3	V	
Input voltage 'H' level	VIH	0.7VDDIO	-	VDDIO	V	
Input voltage 'L' level	VIL	VSS	-	0.3VDDIO	V	
Power supply current	IVDD	-	10	15	mA	
TFT gate on voltage	VGH	-	-	-	V	
TFT gate off voltage	VGL	-	-	-	V	
Analog power supply voltage	AVDD	-	-	-	V	
Differential input common mode voltage	Vcom	-	-	-	V	

4. BACKLIGHT CHARACTERISTICS

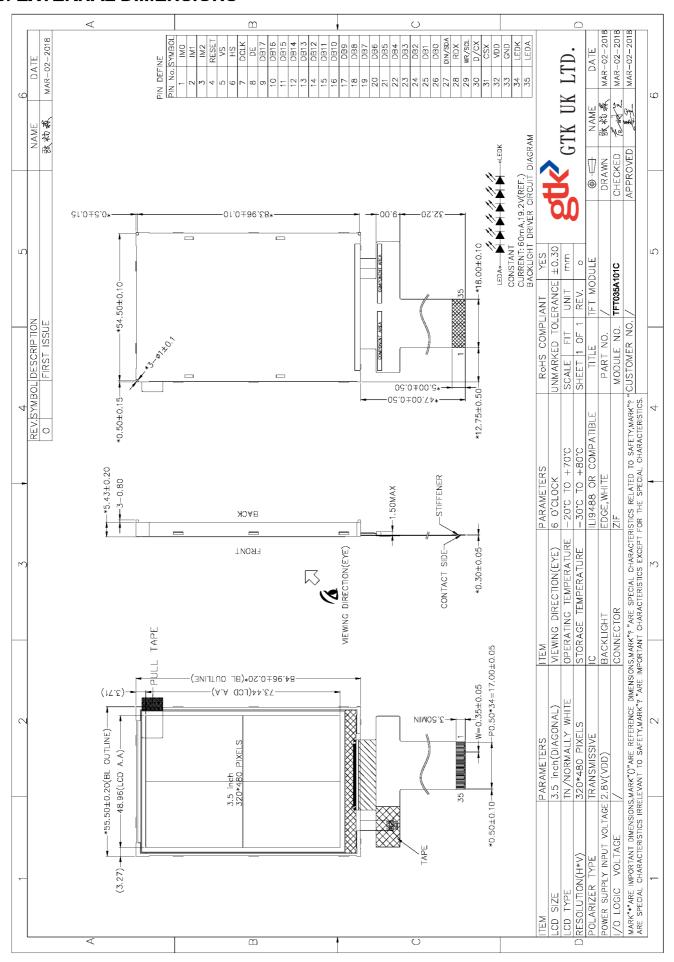
(at Ta=25°C.RH=60%)

at 1a=25 0;1t11=0070j											
Item	Symbol	Min.	Тур.	Max.	Unit	Note					
LED forward voltage	VF	-	19.2	-	V	IF=60mA					
LED forward current	IF	-	60	-	mA						
LED power consumption	PLED	-	1.152	-	W	Note1					
Number of LED	-		6		PCS						
Connection mode	-	6	in series		1						
LED life-time	-	20000	-	-	Hrs	Note2					

Note1 : Calculator value for reference : IF*VF = PLED

Note2 : The LED life-time define as the estimated time to 50% degradation of initial brightness at Ta=25°C and IF =60mA. The LED lifetime could be decreased if operating IF is larger than 60mA.

5. EXTERNAL DIMENSIONS



6. ELECTRO-OPTICAL CHARACTERISTICS

Item	Symbol	Condition	Min.	Тур.	Max.	Unit	Remark	Note	
Response time	Tr+ Tf		-	20	40	ms	FIG.1	Note 4	
Contrast ratio	Cr	-	-	500	-	-	FIG.2	Note 1	
Surface luminance	Lv	θ=0°	950	1100	-	cd/m2	FIG.2	Note 2	
Luminance uniformity	Yu	θ=0°	75	80	-	%	FIG.2	Note 3	
NTSC	-	θ=0°	-	60	-	%	FIG.2	Note 5	
	θ	∅=90°	50	60	-	deg	FIG.3		
Viouing angle		∅=270°	50	60	-	deg	FIG.3	Note 6	
Viewing angle		lie 0	∅=0°	60	70	-	deg	FIG.3	Note 6
		∅=180°	60	70	-	deg	FIG.3		
	Red x			TBD		-			
	Red y			TBD		_			
	Green x	θ=0°		TBD		-			
CIE (x,y)	Green y	Ø=0°	Тур	TBD	Тур	-	FIG.2	Note 5	
chromaticity	Blue x	7	-0.04	TBD	+0.04	-	CIE1931	Note 5	
	Blue y	1a-25 C		TBD		-			
	White x			TBD		-			
	White y			TBD		-			

Note1.Definition of contrast ratio

Contrast ratio(Cr) is defined mathematically by the following formula.

For more information see FIG.2.

Contrast ratio= Luminance measured when LCD on the "White" state Luminance measured when LCD on the "Black" state

Measured at the center area of the LCD

Note2.Definition of surface luminance

Surface luminance is the luminance with all pixels displaying white.

For more information see FIG.2.

Lv = Average Surface Luminance with all white pixels(P1,P2,P3,,Pn)

Note3.Definition of luminance uniformity

The luminance uniformity in surface luminance is determined by measuring luminance at each test position 1 through n, and then dividing the maximum luminance of n points luminance by minimum luminance of n points luminance. For more information see FIG.2.

 $Yu = \frac{\text{Minimum surface luminance with all white pixels (P1,P2,P3,.....,Pn)}}{\text{Maximum surface luminance with all white pixels (P1,P2,P3,.....,Pn)}}$

Note4. Definition of response time

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time (T_{ON}) is the time between photo detector output intensity changed from 90% to 10%. And fall time (T_{OFF}) is the time between photo detector output intensity changed from 10% to 90%. For additional information see FIG1.

Note5. Definition of color chromaticity (CIE1931)

CIE (x,y) chromaticity, The x,y value is determined by screen active area center position P5. For more information see FIG.2.

Note6. Definition of viewing angle

Viewing angle is the angle at which the contrast ratio is greater than 10. angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface. For more information see FIG.3.

For viewing angle and response time testing, the testing data is base on Autronic-Melchers's ConoScope or DMS series Instruments or compatible. For contrast ratio, Surface Luminance, Luminance uniformity and CIE, the testing data is base on TOPCON's BM-5or BM-7 photo detector or compatible.

FIG.1. The definition of response Time

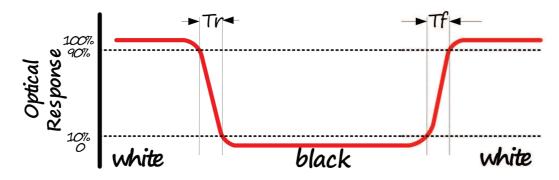


FIG.2. Measuring method for contrast ratio, surface luminance, luminance uniformity, CIE (x,y) chromaticity

Size : S≤5"(see Figure a) A : 5 mm B : 5 mm H,V : Active area

Light spot size \varnothing =5mm(BM-5) or \varnothing =7.7mm (BM-7)50cm distance or

compatible distance from the LCD surface to detector lens.

test spot position : see Figure a.

measurement instrument: TOPCON's luminance meter BM-5 or

BM-7 or compatible (see Figure c).

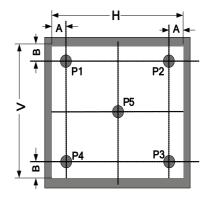


Figure a

Size : 5" \leq S \leq 12.3"(see Figure b)

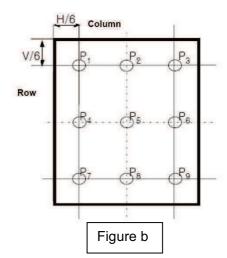
H,V: Active area

Light spot size \varnothing =5mm(BM-5) or \varnothing =7.7mm (BM-7)50cm distance or compatible distance from the LCD surface to detector lens.

test spot position : see Figure b.

measurement instrument: TOPCON's luminance meter BM-5 or

BM-7 or compatible (see Figure c).



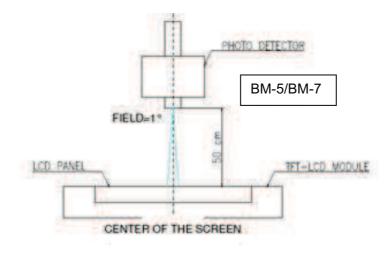
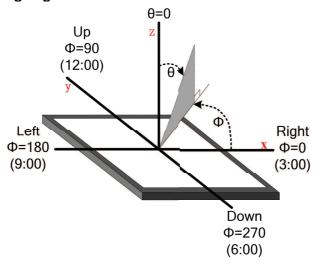


Figure c

FIG.3. The definition of viewing angle



7. INTERFACE DESCRIPTION

TFT Module Interface description

TFT Module	Interface de	scription								
Interface No.	Name	I/O or connect to				Description				
			IM2	IM1	IM0	Interface				
			0	0	0	MIPI-DBI Type B 18-bit bus (DB_EN = 0)				
			0	0 0 1 MIPI-DBI Type B 9-bit bus						
1-3	IM0-IM2		0							
1-3	IIVIU-IIVIZ	I	0	1	1	MIPI-DBI Type B 8-bit bus				
			1	0	1	MIPI-DBI Type C Option 1 (3-line SPI)				
			1	1	0	MIPI-DBI Type C Option 3 (4-line SPI)				
					•					
4	RESET	ı	Chip	reset p	oin("Lo	w Active")This signal will reset the driver and				
4	RESET	I	it mus	st be a	pplied	to properly initialize the chip.				
5	VS	I	Fram	e sync	hroniz	ing signal for RGB interface operation.				
6	HS	I	Line synchronizing signal for RGB interface operation.							
7	DCLK	I	Dot c	lock si	gnal fo	r RGB interface operation.				
8	DE	I	Data	enable	signa	I for RGB interface operation.				
9-26	DB17-DB0	ı	18-bit parallel bi-directional data bus for MCU system and RGB							
9-20	טפט-11סט	Į.	interfa	nterface mode						
27	DIN/SDA	I/O	Seria	I in/out	signa					
28	RDX	I	Serve	es as a	reads	signal .				
29	WR/SCL	1				vrite signal				
29	VVIVOCE	ı	SCL:/	As seri	al cloc	k when operate in the serial interface				
			1			election pin.				
30	D/CX	I	_	Comn						
				Paran						
					input s	0				
31	CSX	l	Low:The chip is selected and accessible							
			High:The chip is not selected and not accessible							
32	VCC	Р		r supp						
33	GND	Р		r Grou						
34	LEDA	Р	Powe	r for L	ED ba	cklight(Cathode)				
35	LEDK	Р	Powe	r for L	ED ba	cklight(Anode)				
		l								

8. AC CHARACTERISTICS

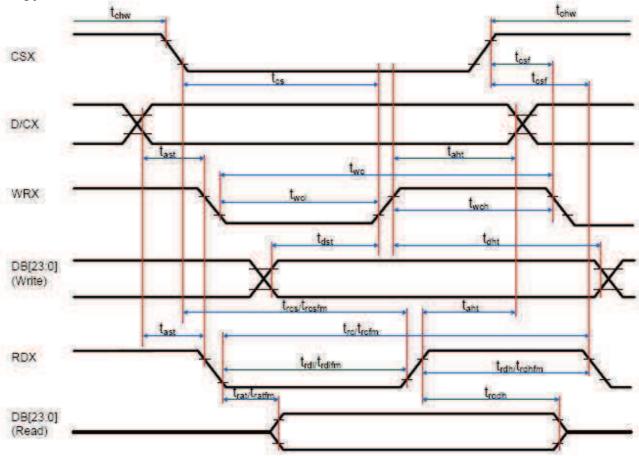
The ILI9488 supports MIPI DBI, DPI, and DBI supports (8-/9-/16-/18-/24-bit interface) Parallel Interface (TypeB) and Serial Interface (Type C). The interface mode can be selected by IM [2:0] pins, as shown in Table 3 below

Table 3: Interface Selection

IM2	IM1	IMO	Interface	Data	Pins in Use
IIVIZ	IIVI I	IIVIO	menace	Command/Parameter	GRAM
0	0	0	DBI Type B 24-bit (DB_EN = 1)	DB [7:0]	DB [23:0]: 24-bits Data
0	0	0	DBI Type B 18-bit (DB_EN = 0)	DB [7:0]	DB [17:0]: 18-bits Data
0	0	1	DBI Type B 9-bit	DB [7:0]	DB [8:0]: 9-bits Data
0	1	0	DBI Type B 16-bit	DB [7:0]	DB [15:0]: 16-bits Data
0	1	1	DBI Type B 8-bit	DB [7:0]	DB [7:0]: 8-bits Data
1	0	1	DBI Type C Option 1 (3-line SPI)	SDA/SDO	Mi
1	1	0	DSI	MIPI_DATA_P, MIPI_DA	Control of the Contro
1	1	1	DBI Type C Option 3 (4-line SPI)	SDA/SDO	

Note:DBI Type B 24-bit and DSI interface are not connect.

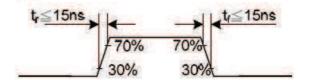
DBI Type B interface characteristic



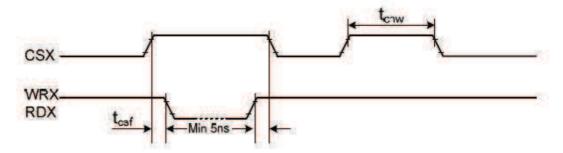
Signal	Symbol	Parameter	min	max	Unit	Description	
DCX	tast	Address setup time	0	2	ns		
DCX	that	Address hold time (Write/Read)	0		ns		
	tchw	CSX "H" pulse width	0		ns) (\$	
	tos	Chip Select setup time (Write)	15	***	ns	on Off	
CSX	trcs	Chip Select setup time (Read ID)	45		ns		
	trosfm	Chip Select setup time (Read FM)	355	*	ns	·	
7	tesf	Chip Select Wait time (Write/Read)	0		ns		
	two	Write cycle	40	34	ns	2	
WRX	twrh	Write Control pulse H duration	15	**	ns		
	twrl	Write Control pulse L duration	15	2	ns	61 (6	
erene il cora	trcfm	Read Cycle (FM)	450		ns		
RDX (FM)	trdhfm	Read Control H duration (FM)	90	- #	ns	When read from Frame Memory	
12-1-4-1-1-2	trdlfm	Read Control L duration (FM)	355	- 27	ns	Memory	
	trc	Read cycle (ID)	160	*	ns		
RDX (ID)	trdh	Read Control pulse H duration	90	*	ns	When read ID data	
7	trdl	Read Control pulse L duration	45	- #	ns	9	
DB [23:0],	tdst	Write data setup time	10	2	ns		
DB [17:0],	tdht	Write data hold time	10	26	ns		
DB [15:0].	trat	Read access time	8 24	40	ns	For maximum, CL=30pF For minimum, CL=8pF	
DB [8:0],	tratfm	Read access time	2	340	ns	TOT THINKING II, OLEOPE	
DB [7:0]	trod	Read output disable time	20	80	ns		

Notes:

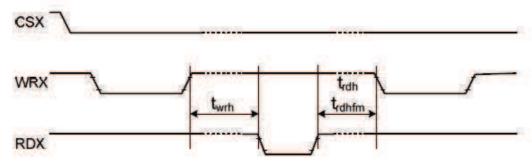
- 1. Ta = -30 to 70 °C, IOVCC = 1.65V to 3.3V, VCI = 2.5V to 3.3V, AGND = DGND = 0V
- 2. Logic high and low levels are specified as 30% and 70% of IOVCC for input signals.
- 3. Input signal rising time and falling time:



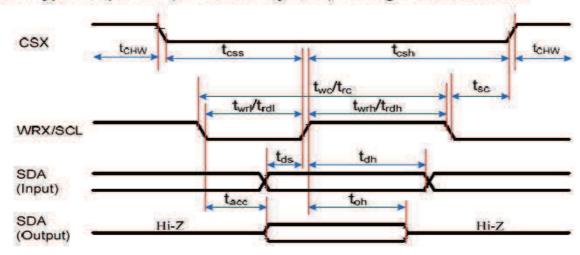
4. The CSX timing:



5. The Write to Read or the Read to Write timing:

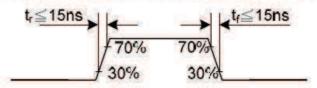


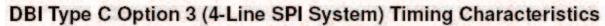
DBI Type C Option 1 (3-Line SPI System) Timing Characteristics

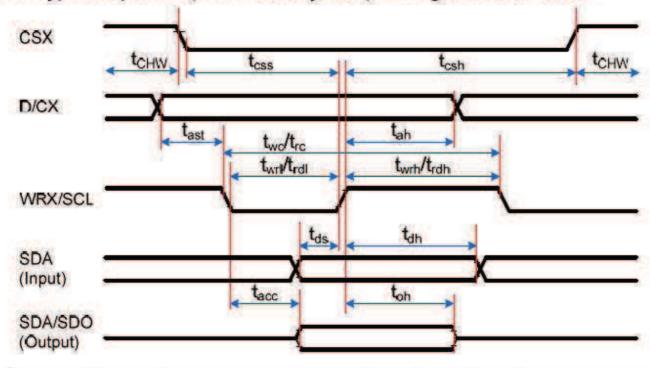


Signal	Symbol	Parameter	min	max	Unit	Description	
	tsc	SCL-CSX	15	(20)	ns		
csx	tchw	CSX H Pulse Width	40		ns		
CSX	tcss	Chip select time (Write)	60	12	ns		
	tosh	Chip select hold time (Read)	65	150	ns		
	twc	Serial Clock Cycle (Write)	66	9	ns		
	twrh	SCL H Pulse Width (Write)	15	200	ns		
0.01	twrl	SCL L Pulse Width (Write)	15	380	ns		
SCL	trc	Serial Clock Cycle (Read)	150	949 7	ns	2 4	
	trdh	SCL H Pulse Width (Read)	60	FIRE	ns		
	trdl	SCL L Pulse Width (Read)	60	(20)	ns		
SDA	tds	Data setup time (Write)	10		ns		
(Input)	tdh	Data hold time (Write)	10	150	ns		
SDA/SDO	tacc	Access time (Read)	10	50	ns	For maximum CL=30pl	
(Output)	toh	Output disable time (Read)	15	50	ns	For minimum CL=8pF	

Note: Ta = -30 to 70 °C, IOVCC = 1.65V to 3.6V, VCI = 2.5V to 3.6V, AGND = DGND = 0V, T = 10+/-0.5ns





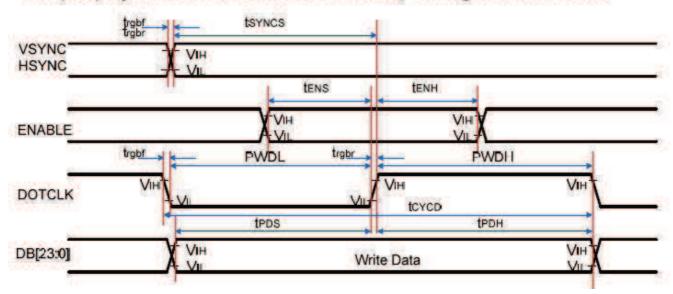


Signal	Symbol	Parameter	min	max	Unit	Description
- 0	tcss	Chip select time (Write)	15		ns	
CSX	tcsh	Chip select hold time (Read)	15		ns	
	tCHW	CS H pulse width	40		ns	
	twc	Serial clock cycle (Write)	50	975	ns	
	twrh	SCL H pulse width (Write)	10		ns	
0.01	twrl	SCL L pulse width (Write)	10	*	ns	
SCL	trc	Serial clock cycle (Read)	150	¥	ns	
	trdh	SCL H pulse width (Read)	60	34	ns	2
-	trdl	SCL L pulse width (Read)	60	25	ns	- E
D/CX	tas	D/CX setup time	10		ns	
DrCX	tah	D/CX hold time (Write/Read)	10		ns	
SDA	tds	Data setup time (Write)	10	*	ns	A.
(Input)	tdh	Data hold time (Write)	10	-	ns	
SDA/SDO	tacc	Access time (Read)	10	50	ns	For maximum CL=30pF
(Output)	tod	Output disable time (Read)	15	50	ns	For minimum CL=8pF

Notes:

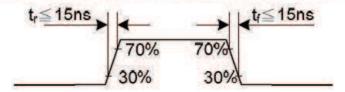
- 1. Ta = -30 to 70 °C, IOVCC = 1.65V to 3.3V, VCI = 2.5V to 3.3V, AGND = DGND = 0V, T = 10+/-0.5ns.
- 2. Does not include signal rising and falling times.

DPI (Display Parallel 16-/18-/24-bit interface) Timing Characteristics



Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC/	tsyncs	VSYNC/HSYNC setup time	15	2	ns	
HSYNC	tsynch	VSYNC/HSYNC hold time	15	<u>.</u>	ns	
ENABLE	tens	ENABLE setup time	15	2 84	ns	
	tenh	ENABLE hold time	15	2	ns	16-/18-/24-bit bus RGB interface mode
DD 100-01	tpos	Data setup time	15		ns	
DB [23:0]	tppH	Data hold time	15	13	ns	
	PWDH	DOTCLK high-level period	20	¥	ns	
DOTCLK	PWDL	DOTCLK low-level period	20	- 2	ns	
DOTCLK	toyop	DOTCLK cycle time	50	8	ns	
	t _{rgbr} , t _{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time		15	ns	

Note: Ta = -30 to 70 °C, IOVCC = 1.65V to 3.3V, VCI = 2.5V to 3.3V, AGND = DGND = 0V

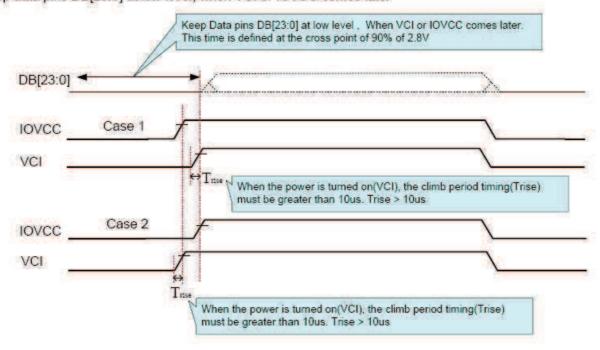


9. POWER SEQUENCE

IOVCC and VCI can be applied or powered down in any order. During the Power Off sequence, if the LCD is in the Sleep Out mode, VCI and IOVCC must be powered down with a minimum of 120msec. If the LCD is in the Sleep In mode, VCI and IOVCC can be powered down with a minimum of 0msec after the RESX has been released. CSX can be applied at any time or can be permanently grounded. RESX has high priority over CSX.

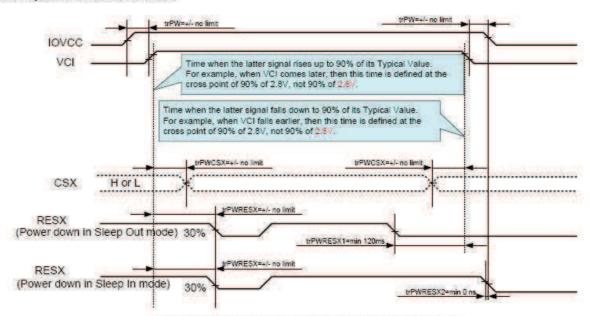
Notes:

- 1. There will be no damage to the ILI9488 if the power sequences are not met.
- 2. There will be no abnormal visible effects on the display panel during the Power On/Off Sequence.
- 3. There will be no abnormal visible effects on the display between the end of the Power On Sequence and before receiving the Sleep Out command, and also between receiving the Sleep In command and the Power Off Sequence.
- 4. If the RESX line is not steadily held by the host during the Power On Sequence as defined in Sections 11.1 and 11.2, then it will be necessary to apply the Hardware Reset (RESX) after the completion of the Host Power On Sequence to ensure correct operations. Otherwise, all the functions are not guaranteed.
- 5. When the power is turned on, the climb period timing(Trise) must be greater than 10us.
- 6. Keep data pins DB[23:0] at low level, when VCI or IOVCC comes later



Case 1 – NRESET line is held high or unstable by host at power on

If the RESX line is held High or unstable by the host during Power On, then Hardware Reset must be applied after both VCI and IOVCC have been applied. Otherwise, the correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.



trPWRESX1 is applied to RESX falling in the Sleep Out Mode trPWRESX2 is applied to RESX falling in the Sleep In Mode

Note: Unless otherwise specified, timings herein show the cross point at 50% of the signal power level.

10. RELIABILITY TEST CONDITIONS

No.	Test item	Test con	dition	Inspection after test
10.1	High temperature storage test	+80C/240 hours		
10.2	Low temperature storage test	-30°C/240 hours	-30°C/240 hours	
10.3	High temperature operating test	+70°C/120 hours		
10.4	Low temperature operating test	-20°C/120 hours		Inspection after
10.5	Temperature cycle storage test	-30°C ~ 25°C ~ +80°C/10cycles (30min) (10min) (30min)		2~4hours storage at room temperature, the sample shall be free
10.6	High temperature high humidity test	+50°C*90% RH/120	+50°C*90% RH/120 hours	
10.7	Vibration test	Frequency : 250 r/mi Amplitude : 1 inch Time: 45min		
		Drop direction: 1 corner/3 edges/6 s	Non-display,abnormal-d isplay,missing lines, Short lines,ITO	
		Packing weight(kg)	Drop height(cm)	corrosion;
10.8	Drop test	<11	80±1.6	3.Visual defect : Air bubble in the LCD,Seal
		11≦G<21	60±1.2	leak,Glass crack.
		21≦G<31	50±1.0	
		31 ≦ G<40	40±0.8	
10.9	ESD test	Air discharge: ±8KV, Contact discharge: ±		

Remark:

- 1. The test samples should be applied to only one test item.
- 2. Sample size for each test item is 3~5pcs.
- 3. For High temperature high humidity test, Pure water(Resistance>10M Ω) should be used.
- 4.In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.
- 5.B/L evaluation should be excepted from reliability test with humidity and temperature: Some defects such as black spot/blemish can happen by natural chemical reaction with humidity and Fluorescence B/L has.
- 6.Failure judgment criterion: Basic specification, Electrical characteristic, Mechanical characteristic, Optical characteristic.

11. INSPECTION CRITERION

11.1 Objective

The TFT test criterion are set to formalize TFT quality standards for GTK with reference to those of the customer for inspection, release and acceptance of finished TFT products in order to guarantee the quality of TFT products required by the customer.

11.2. Scope

The criterion is applicable to all the TFT products manufactured by GTK.

11.3. Equipment for Inspection

Electrical tester, electrical testing machines, vernier calipers, microscopes, magnifiers, anti-static wrist straps, finger cots, labels, tri-phase cold and hot shock machine, constant temperature and humidity chamber, backlight table, ovens for high-low temperature experiments, refrigerators, constant voltage power supply (DC), desk Lamps, etc.

11.4. Sampling Plan and Reference Standards

11.4.1 Sampling plan:

Refer to National Standard GB/T 2828.1---2012/ISO2859-1:1999, level II of normal levels:

Major defect: AQL 0.4 Minor defect: AQL 1.0

11.4.2 GB/T 2828.1---2012/ISO2859-1:1999 Sampling check procedure in count

11.4.3 GB/T 18910. Standard for LCM parts

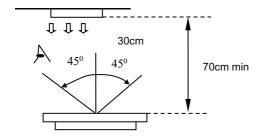
11.4.4 GB/T24213-2008 Basic Environmental Test Procedures for Electrical and Electronic Products

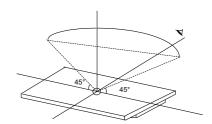
11.4.5 IPC-A-610E Acceptability of Electronic Assemblies

11.5. Inspection Conditions and Inspection Reference

11.5.1 Cosmetic inspection: shall be done normally at $23\pm5^{\circ}$ C of the ambient temperature and $45\sim75\%$ RH of relative humidity, under the ambient luminance between 500lux~1000lux and at the distance of 30cm apart between the inspector's eyes and the LCD panel and normally in reflected light. For backlight LCM, cosmetic inspection shall be done under the ambient luminance less than 100lux with the backlight on.

11.5.2 The TFT shall be tested at the angle of 45°left and right and 0-45° top and bottom as the following picture showing:





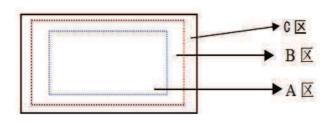
11.5.3 Definition of viewing area(VA)

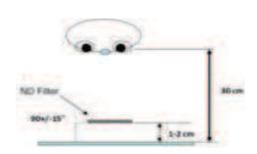
A area : Active area(AA area)
B area : Viewing area(VA area)

C area: Non-viewing area(not viewing after customer assembly)

If there is any appearance viewing defect which do not affect product quality and customer assembly in C area, it's accepted in generally.

The criteria apply to A and B area except chipping and crack.





- 11.5.4 Inspection with naked eyes(exclusive of the inspection of the physical dimensions of defects carried out with magnifiers)
- 11.5.5 ND card use method(refer to right conner image) and scope: Multi-bright dot; Mura(Black/Gray pattern uneven); dark line and so on.
- 11.5.6 Undefined items or other special items, refer to mutual agreement and limited sample. If criterion does not match product specifications/ technical requirement, both should be subject to special inspection criterion agreed by customer.

11.6. Defects and Acceptance Standards

- 11.6.1 Electrical properties test
- 11.6.1.1 Test voltage(V): Refer to the instruction of testers and the product specification or drawing and the display content and parameters and display effects shall conform to the product specification and drawing.
- 11.6.1.2 Current Consumption(I): Refer to approved product specifications or drawings.

11.6.1.3 Function items(Defect category : MA.)

No.	Defects	Descriptions	Pictures	Inspection method/tools	Defect category
11.6.1.3.1	No display /reaction	shows no picture/display in normal connected situation.		Naked eyes/ testers	MA.
11.6.1.3.2	Missing segment	Shows missing lines in normal display		Naked eyes/ testers	MA.
11.6.1.3.3	Dark line	Only visible on gray pattern, 1 or more vertical/horizontal lines:5%ND,not visible,OK	1	Naked eyes/ testers	MA.
11.6.1.3.4	POL angle defect	Not accepted	正常 POL贴反180度后	Naked eyes/ testers	MA.
11.6.1.3.5	Image retention (sticking)	Chess pattern stays for 30mins and change to 50% gray pattern, disappear time <10s, OK; if time>10s, NG		Naked eyes/ testers	MA.
11.6.1.3.6	Flicker	Refer to limit sample if essential or flicker value<-30dB(measured by CA310A); OK		Naked eyes/ CA310A	MA.
11.6.1.3.7	Display abnormal	Not accepted		Naked eyes/ testers	MA.
11.6.1.3.8	Cross-talk	Refer to limited sample	V	Naked eyes/ limited sample	MA.
11.6.1.3.9	Display dim/bright	Refer to limited sample	1	Naked eyes/ limited sample	MA.
11.6.1.3.10	Contrast	Refer to limited sample	1	Naked eyes/ limited sample	MA.
11.6.1.3.11	Huge current	Out of spec, not accepted	1	Ammeter	MA.

	TP			Naked eyes/		ĺ
11.6.1.3.12	function	Not accepted	1	Touch/	MA.	
	defect			test program		

11.6.2 LCD dot/line defect

11.6.2.1 LCD pixel dot defect(defect category : MI.)

Item		Inspection criterio	n
Size	S<5"	5"≤S<10"	10"≤S<15"
Color pixel dot defect(RGB dot)	1	2	2
2 connected bright dot	0	1	1
3 connected bright dot or more	0	0	1
Bright dot quantity	1	2	3
Random dark dot quantity	2	3	4
2 connected dark dot	1	1	2
3 connected dark dot or more	0	0	0
Dark dot quantity	3	4	5
Multi-bright dot		ND 3%hidden, OK	

Remark: 2 bright dots distance DS≥15mm 2 dark dots distance DS≥5mm

- 1) Bright dot: Power on TFT and RGB dot in black display
- 2) Dark dot: Power on TFT and gray or black dot in RGB display
- 3) Multi-bright dot: Power on TFT and fluorescent tiny dot in black display(only visible in black display)

11.6.2.2 LCD appearance dot defect (defect category : MI.)

No.	ltom		Ins	spection c	riterion		Picture	Inspection
NO.	Item	Si	ze	S<5"	5"≤S<10"	10"≤S<15"	Picture	method/tools
		D≤0).15	Not count	Not count	D≤0.2mm		
		0.15<	D≤0.25	3	3	Not count	1 b	Naked eyes
		0.25<	D≤0.30	1	2	0.2~0.35mm	• a •	/film card
	Dot defect	0.30<	0.30 <d≤0.35< td=""><td>1</td><td>Q'ty ≤ 4</td><td></td><td>/magnifier</td></d≤0.35<>		1	Q'ty ≤ 4		/magnifier
11.6.2.2.1	(black dot,	0.35<	0.35 <d≤0.50< td=""><td>0</td><td>1</td><td>D=(a+b)/2</td><td>/magniner</td></d≤0.50<>		0	1	D=(a+b)/2	/magniner
	white dot)	D>0.5		0	0	0		
		Remark:	D≤0.15m	m, not cou	nt.Multi-dot	as bulk is not	accepted.	
		Count do	t quantity≤	5				
		2 round d	ots or line	ar dots in	1 cm is judo	ged as multi-d	ot.	
		Length	Width	S<5"	5"≤S<10"	10"≤S<15"		
		(mm)	(mm)	0 10	0 20 110	10 20 110		
		Not	W≤0.03	Accepted	Accepted	Accepted	100	
		count				, 1000p100.		
		L≤5	0.03≤W	3	3	Not count	1 *	Naked eyes
	Line		<0.05					/film card
	defect	L≤5	0.05≤W	0	1 3	100	/magnifier	
11.6.2.2.2	(visible		<0.08				1	
	when	L≤8	0.05≤W <0.08	0	0	1		
	power on)	L>8	<0.08 W>0.08	0			1	
			VV>0.08	U			100000000000000000000000000000000000000	
		Remark:						
			•	-		pecial angle ag		
			K/folding/s	scratch but	can not be	touched, no o	control or refe	r to keeping
MODIII E Na		sample.						

	Polarizer	Size(mm)	S<5"	5"≤S<10"	10"≤S<15"		
	convex-	D≤0.20	Not count	Not count	Not count		
	concave	0.20 <d≤0.5< td=""><td>2</td><td>2</td><td>3</td><td></td><td>Naked eyes</td></d≤0.5<>	2	2	3		Naked eyes
11.6.2.2.3	dot defect,	0.50 <d≤0.8< td=""><td>0</td><td>1</td><td>3</td><td>10</td><td>/film card</td></d≤0.8<>	0	1	3	10	/film card
	polarizer	0.8 <d≤1.5< td=""><td>0</td><td>0</td><td>1</td><td>• a •</td><td>/magnifier</td></d≤1.5<>	0	0	1	• a •	/magnifier
	bubble defect	D>1.5mm	0	0	0	00. 80. 00	

No.	Item		Accepte	d criterion(mm)		MA.	MI.
11.6.3.1	ITO conductive side	Х	/	≤1/8L	1		
		Y	Y≤1/6W	1/6W <y≤1 4w<="" td=""><td>1/4W <y< td=""><td></td><td>1</td></y<></td></y≤1>	1/4W <y< td=""><td></td><td>1</td></y<>		1
	Z	Accept	2	2	0		$\sqrt{}$
	Corner chipping	X	/	≤1/6L	/		.1
	(ITO pins position)	Y	Y≤1/2W	1/2W <y≤w< td=""><td>W <y< td=""><td></td><td>$\sqrt{}$</td></y<></td></y≤w<>	W <y< td=""><td></td><td>$\sqrt{}$</td></y<>		$\sqrt{}$
11.6.3.2		Accept	2	1	0		
	2	Corner chipping occurred in sealed edge position as per 6.3.3; at the same time it should not enter into black border of the frame and the corner chipping effect the electric connection position perform as per 6.3.1.					
	Chipping in sealed area (outside chipping)	X	1	≤1/8L	1		
	area (eatelier emphrig)	Y(outside chipping)	Not enter	Enter Y≤H	H <y< td=""><td></td><td></td></y<>		
		Y(inside chipping)	into sealant	Enter Y≤1/2H	1/2H <y< td=""><td></td><td></td></y<>		
11.6.3.3	27	Z	≤T	≤1/2T	/		$\sqrt{}$
	12	Accept	2	1	0		
	Chipping in sealed area (inside chipping)	sealing are in the oppo	a are same site of stage	r and outer chippi . When the chippi e, Y as per the chip andard in 6.3.1	ng occurred		
	Conductive side (back side chipping)	Х	1	≤1/6L	/		
44.00.4	, y	Υ	Y≤1/3W	1/3W <y≤2 3w<="" td=""><td>2/3W <y< td=""><td></td><td></td></y<></td></y≤2>	2/3W <y< td=""><td></td><td></td></y<>		
11.6.3.4	Z	Accept	2	2	0		
	\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	Chipping into ITO side, refer to 6.3.1					

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	Protruding LCD poor cutting and LCD burrs	×	/	≤1/8L	/		
	cutting and LOD build	Υ	≤1/6W	1/6W <y≤1 5w<="" td=""><td>1/5W <y< td=""><td></td><td>ا</td></y<></td></y≤1>	1/5W <y< td=""><td></td><td>ا</td></y<>		ا
11.6.3.5	b	Z	/	/	1		V
		Accept	1	1	1	1	
		The outside drawing.	The outside protruding control as per the tolerance of drawing.				
11.6.3.6	Crack	expand to	inside is NG,	ks without direction , but to outside is C amaged standard)	K		V

Remark:

X means the length of chipping;

Y means the width;

Z means the thickness;

W means the step width of the two glasses;

H means the distance from the glass edge to the sealant inner edge;

T means glass thickness.

11.6.4 Backlight components

No.	Item	Description	Accepted criterion	MA.	MI.
11.6.4.1	No backlight wrong Color	1	Rejected	√	
11.6.4.2	Color deviation	When powered on, the LCD color differs from its sample and found that the color not conforming to the drawing after testing.	Refer to sample and drawing		V
11.6.4.3	Brightness deviation	When powered on, the LCD brightness differs from its sample and is found after testing not conforming to the drawing; or if it conforms to the drawing but the brightness over ±40% than its typical value.	Refer to sample and drawing		√
11.6.4.4	Uneven brightness	Uneven on the same LCD and out of the specification of the drawing. The no specification evenness= (the max value-the min value)/ mean value< 70%.	Refer to sample and drawing		√
11.6.4.5	Spot/line/ scratch	When power on, it has dirty spot, scratches and so on spot and line defects.	Refer to 6.2.2		$\sqrt{}$

11.6.5 Metal frame (Metal Bezel)

No.	Item	Description	Accepted criterion	MA.	MI.
11.6.5.1	Material & surface treatment	Metal frame/surface treatment do not conform to the specifications.	Rejected	V	
11.6.5.2	Tab twist Unconformity /Tab not twisted	Wrong twist method or direction and twist tabs are not twisted as required.	Rejected	~	

11.6.5.3	Bezel paint loss	1.Front surface : Paint peel off and scratch to the		V
11.6.5.4	Bezel scratch	bottom Dot:D≤0.5mm, exceeds 3;		~
11.6.5.5	Painting peel off, discoloration, dent, and scratch	Line:L≤3.0mm,W≤0.05mm exceeds 2; 2.Front dent, air bubble and side with paint peeling off scratch to the bottom Dot: D≤1.0mm, exceeds 3; Line:L≤3.0mm,W≤0.05mm, exceeds 2;	Rejected	√
11.6.5.6	Burr	Burr(s) on metal bezel is so long as to get into viewing area.	Rejected	~

11.6.6 FPC

No.	Item	Description	Accepted criterion	MA.	MI.
11.6.6.1	Model &P/N	Material model & P/N	Keep the same with drawing and technical requirement	V	
11.6.6.2	Dimension/ position	Dimension in drawing spec H	f≤1/3w, h ≤1/3H, dimension in drawing spec-> OK Conducive material and ITO/PDA connective area must over than 1/2. Entire dimension must be in spec tolerance.		√
11.6.6.3	FPC appearance	Hot pressing material get broken, folding line open; FPC golden finger oxidate, broken ,scratch ,foreign material which cause line short	Broken length<2mm; FPC line is OK- > Accepted Crack and line broken->Rejected		V
11.6.6.4	FPC burr	Burr near FPC edge area	When cover line and burr length ≤1.0mm->Accepted		V
11.6.6.5	FPC falling off	FPC bonding area falling off; silica gel breaking	Rejected		V
11.6.6.6	Sealant missing ITO line	Sealant is not covered all ITO line	Rejected	V	
11.6.6.7	Missing sealant	No sealant	Rejected	√	
11.6.6.8	Sealant	Sealant height ->product total height	Rejected	√	

11.6.7 SMT

No.	Item	Description	Accepted criterion	MA.	MI.
11.6.7.1	Soldering bridge	Solder between adjacent pads and components	Rejected		V
11.6.7.2	Solder ball/splash	Solder ball/tin dross causing short circuit at the solder point. There are active solder ball and splash.	Rejected		V
11.6.7.3	Soldering excursion	Soldering slant > 1/3 soldering pad 「學學表現	Rejected		V
11.6.7.4	Component wrong	Component on PCB differs with drawing: wrong one, extra one,lack one,opposite polarity	Rejected	V	
	attaching	JUMP short circuit on PCB: extra soldering ,lack soldering.	Rejected	√	
11.6.7.5	Component falling off	Soldering but component is missing	Rejected	$\sqrt{}$	
11.6.7.6	Wrong component	Component model/spec differs from product specification	Rejected	√	

11.6.8 General Appearance

No.	Item	Description	Accepted criterion	MA.	MI.
11.6.8.1	Dimension	According to drawing	Accepted	√	
11.6.8.2	Surface stain	Defect mark or label are not removed residual glue, and finger print,etc;	Rejected		√
11.6.8.3	Assembly foreign material	Dot/linear stain after assembly backlight and diffuse film TP assembly fogy stain	Invisible when power on->OK Refer to 6.2.2 dot/line spec		√
11.6.8.4	Mixture	Different model product in the same shipment	Rejected	$\sqrt{}$	
11.6.8.5	Product mark	Missing, unclear, incorrect, or misplaced part	Rejected		V
11.6.8.6	Componen t mark	Silk screen mark clear, resistance measured value in spec	Accepted (Refer to customer special requirement)		√
11.6.8.7	Newton's rings	Area<1/6 screen area quantity≤1	Accepted		1
11.6.8.8	Mura	1.In black display ND 3% invisible ->OK; visible->NG 2.Naked eyes inspection RGB display invisible Black display, area<1/4 screen area	Refer to limited sample		√

11.6.8.9	Light leak	1.LCD edge(near backlight) shadow by LCD lamps irregular illuminate 2.Judge in black/white/gray display (slight leaky is yellowish,greenish, blueish ->NG); Tape 浮起漏光	Refer to limited sample	√	
11.6.8.10	Polarizer	1.Polarizer slant.Cover VA and not over LCD edge 2.No unmovable stain or finger print in polarizer VA 3.Bubble/warped but not enter VA	Accepted	V	
11.6.8.11	TP defect	1.TP crack 2.TP stain(fogy& unremovable) 3.TP glue overflow to VA	Rejected	V	

Remark:

Anything which is not clearly defined in $6.5\sim6.8$ should refer to IPC-A-610E.Consumer Electronics, Non-consumer Electronics refer to I grade and Industrial, Automobile refer to II grade.

11.7 Others

Items not specified in this document or released on compromise should be inspected with reference to mutual agreement and limit samples.

12. HANDLING PRECAUTIONS

12.1 Mounting method

The LCD module consists of two thin glass plates with polarizes which easily be damaged. And since the module in so constructed as to be fixed by utilizing fitting holes in the printed circuit board.

Extreme care should be needed when handling the LCD modules.

12.2 Caution of LCD handling and cleaning

When cleaning the display surface, Use soft cloth with solvent

[recommended below] and wipe lightly:

- .lsopropyl alcohol
- Ethyl alcohol

Do not wipe the display surface with dry or hard materials that will damage the polarizer surface.

Do not use the following solvent:

- .Water
- Aromatics

Do not wipe ITO pad area with the dry or hard materials that will damage the ITO patterns

Do not use the following solvent on the pad or prevent it from being contaminated:

- Soldering flux
- •.Chlorine (CI), Sulfur (S)

If goods were sent without being silicon coated on the pad, ITO patterns could be damaged due to the corrosion as time goes on.

If ITO corrosion happen by miss-handling or using some materials such as Chlorine (CI), Sulfur (S) from customer, Responsibility is on customer.

12.3 Caution against static charge

The LCD module use C-MOS LSI drivers, so we recommended that you:

Connect any unused input terminal to Vdd or Vss, do not input any signals before power is turned on, and ground your body, work/assembly areas, assembly equipment to protect against static electricity.

12.4 Packing

Module employ LCD elements and must be treated as such.

- Avoid intense shock and falls from a height.
- •. To prevent modules from degradation, do not operate or store them exposed direct to sunshine or high temperature/humidity.

12.5 Caution for operation

- •.It is an indispensable condition to drive LCD's within the specified voltage limit since the higher voltage then the limit cause the shorter LCD life.
- •.An electrochemical reaction due to direct current causes LCD's undesirable deterioration, so that the use of direct current drive should be avoided.
- •.Response time will be extremely delayed at lower temperature then the operating temperature range and on the other hand at higher temperature LCD's how dark color in them. However those phenomena do not mean malfunction or out of order with LCD's, which will come back in the specified operation temperature.
- •.If the display area is pushed hard during operation, some font will be abnormally displayed but it resumes normal condition after turning off once.
- •.A slight dew depositing on terminals is a cause for electro-chemical reaction resulting in terminal open circuit.
- •. Usage under the maximum operating temperature, 50%Rh or less is required.
- •.When fixed patterns are displayed for a long time, remnant image is likely to occur.

12.6 Storage

In the case of storing for a long period of time for instance, for years for the purpose or replacement use, the following ways are recommended.

- •.Storing in an ambient temperature 10°C to 30°C, and in a relative humidity of 45% to 75%. Don't expose to sunlight or fluorescent light.
- •. Storing in a polyethylene bag with the opening sealed so as not to enter fresh air outside in it. And with no desiccant.
- •.Placing in a dark place where neither exposure to direct sunlight nor light's keeping the storage temperature range.
- •. Storing with no touch on polarizer surface by the anything else.

It is recommended to store them as they have been contained in the inner container at the time of delivery from us.

12.7 Safety

- •.It is recommendable to crash damaged or unnecessary LCD's into pieces and wash off liquid crystal by either of solvents such as acetone and ethanol, which should be burned up later.
- •. When any liquid leaked out of a damaged glass cell comes in contact with your hands, please wash it off well with soap and water.

13. PRECAUTION FOR USE

- **13.1** A limit sample should be provided by the both parties on an occasion when the both parties agreed its necessity. Judgment by a limit sample shall take effect after the limit sample has been established and confirmed by the both parties.
- **13.2** On the following occasions, the handing of problem should be decided through discussion and agreement between responsible of the both parties.
- •. When a question is arisen in this specification.
- •. When a new problem is arisen which is not specified in this specifications.
- •.When an inspection specifications change or operating condition change in customer is reported to GTK, and some problem is arisen in this specification due to the change.
- •. When a new problem is arisen at the customer's operating set for sample evaluation in the customer site.

14. PACKING SPECIFICATION

Please consult our technical department for detail information.