



**SPECIFICATION
FOR
E-PAPER MODULE**

MODULE No. : EPA122250A101A

CUSTOMER APPROVAL:

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	SIGNATURE	DATE
PREPARED BY		2017.8.8
CHECKED BY		2017.8.8
APPROVED BY		2017.8.8

Notes :

- 1、 Please contact GTK before assigning your product based on this module specification.
- 2、 To improve the quality of product, and this product specification is subject to change without any notice.

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1. Over View

EPA122250A101A is an Active Matrix ophoretic Display (AM EPD),owith interface and a reference system design. The 2.13inch active area contains 250×122 pixels. The module is a TFT-array driving electrophoresis display, with integrated circuits including gate driver, source driver, MCU interface, timing controller, oscillator, DC-DC, SRAM, LUT, VCOM. Module can be used in portable electronic devices, such as Electronic Shelf Label (ESL) System.

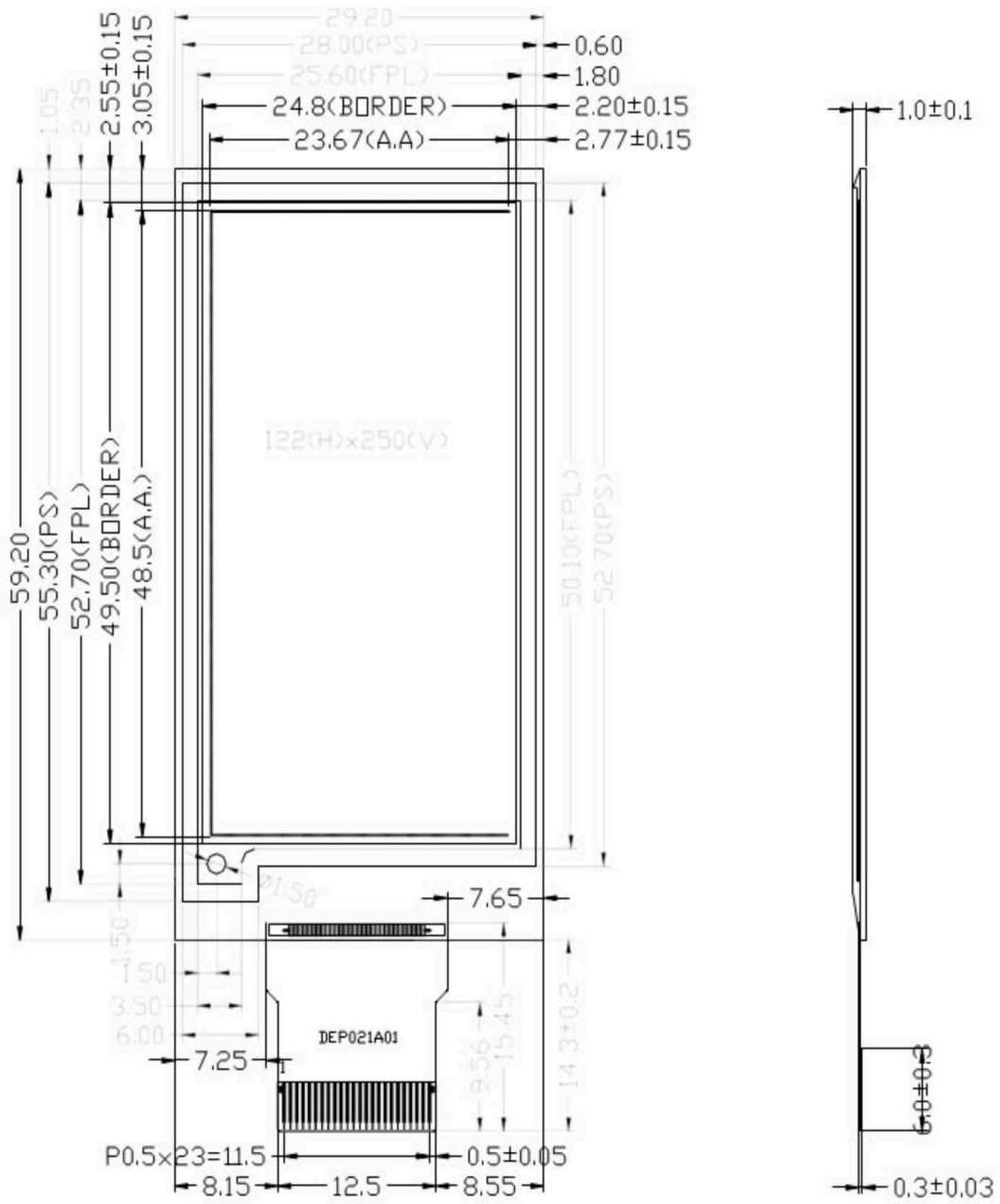
2. Features

- ◆250×122 pixels display
- ◆High contrast High reflectance
- ◆Ultra wide viewing angle Ultra low power consumption
- ◆Pure reflective mode
- ◆Bi-stable display
- ◆Commercial temperature range
- ◆Landscape portrait modes
- ◆Hard-coat antiglare display surface
- ◆Ultra Low current deep sleep mode
- ◆On chip display RAM
- ◆Waveform can stored in On-chip OTP or written by MCU
- ◆Serial peripheral interface available
- ◆On-chip oscillator
- ◆On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- ◆I²C signal master interface to read external temperature sensor
- ◆Support partial update mode

3. Mechanical Specification

Parameter	Specifications	Unit	Remark
Screen Size	2.13	Inch	
Display Resolution	122(H)×250(V)	Pixel	DPI:130
Active Area	23.67×48.50	mm	
Pixel Pitch	0.194×0.194	mm	
Pixel Configuration	Rectangle		
Outline Dimension	29.2(H)×59.2 (V) ×1.05(D)	mm	
Weight	3.2±0.5	g	

4. Mechanical Drawing of EPD Module



5. Input/output Pin Assignment

No.	Name	I/O	Description	Remark
1	NC		Do not connect with other NC pins	Keep Open
2	GDR	O	N-Channel MOSFET Gate Drive Control	
3	RESE	I	Current Sense Input for the Control Loop	
4	VGL	C	Negative Gate driving voltage	
5	VGH	C	Positive Gate driving voltage	
6	NC		Do not connect with other NC pins	Keep Open
7	Tout1	O	For Test	Keep Open
8	BS1	I	Bus Interface selection pin	Note 5-5
9	BUSY	O	Busy state output pin	Note 5-7
10	RES#	I	Reset signal input. Active Low.	Note 5-3
11	D/C#	I	Data /Command control pin	Note 5-2
12	CS#	I	Chip select input pin	Note 5-1
13	D0	I	Serial Clock pin (SPI)	
14	D1	I	Serial Data pin (SPI)	
15	VDDIO	P	Power Supply for interface logic pins It should be connected with VCI	
16	VCI	P	Power Supply for the chip	
17	VSS	P	Ground	
18	VDD	C	Core logic power pin VDD can be regulated internally from VCI. A capacitor should be connected between VDD and VSS	
19	VPP	P	FOR TEST	Keep Open
20	VSH	C	Positive Source driving voltage	
21	VGH	C	Positive Gate driving voltage	
22	VSL	C	Negative Source driving voltage	
23	PREVGL	C	Power Supply pin for VCOM, VGL and VSL	
24	VCOM	C	VCOM driving voltage	

I = Input Pin, O =Output Pin, /O = Bi-directional Pin (Input/output), P = Power Pin, C = Capacitor Pin

Note 5-1: This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW.

Note 5-2: This pin is (D/C#) Data/Command control pin connecting to the MCU in 4-wire SPI mode. When the pin is pulled HIGH, the data at SDA will be interpreted as data. When the pin is pulled LOW, the data at SDA will be interpreted as command.

Note 5-3: This pin (RES#) is reset signal input. The Reset is active low.

Note 5-4: This pin is Busy state output pin. When Busy is High, the operation of chip should not be interrupted, command should not be sent. The chip would put Busy pin High when -Outputting display waveform -Communicating with digital temperature sensor

Note 5-5: Bus interface selection pin

BS1 State	MCU Interface
L	4-lines serial peripheral interface(SPI) - 8 bits SPI
H	3- lines serial peripheral interface(SPI) - 9 bits SPI

6. Electrical Characteristics

6.1 Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Logic supply voltage	VCI	-0.5 to +4.0	V
Logic Input voltage	VIN	-0.5 to VCI +0.5	V
Logic Output voltage	VOUT	-0.5 to VCI +0.5	V
Operating Temp range	TOPR	0 to +50	°C.
Storage Temp range	TSTG	-25 to+70	°C.

Note:

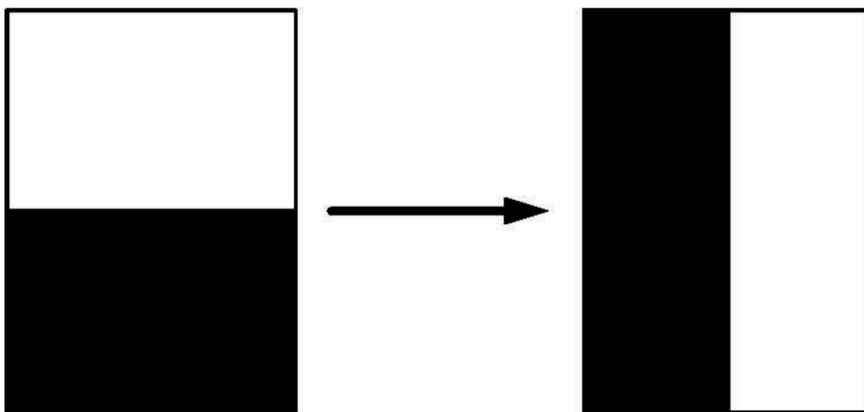
- 1.Maximum ratings are those values beyond which damages to the device may occur.
- 2.Functional operation should be restricted to the limits in the Panel DC Characteristics tables.
3. Optimal operating temperature range: 0-30°C(@1pixel) 30~70%RH
4. The optimal storage environment: 23±2°C 55±10%RH.

6.2 Panel DC Characteristics

The following specifications apply for: VSS=0V, VCI=3.0V, TOPR =25°C.

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
Single ground	VSS	-		-	0	-	V
Logic supply voltage	VCI	-	VCI	2.2	3.0	3.7	V
Core logic voltage	VDD		VDD	1.7	1.8	1.9	V
High level input voltage	VIH	-	-	0.8 VCI	-	-	V
Low level input voltage	VIL	-	-	-	-	0.2 VCI	V
High level output voltage	VOH	IOH = -100uA	-	0.9 VCI	-	-	V
Low level output voltage	VOL	IOL = 100uA	-	-	-	0.1 VCI	V
Typical power	PTYP	VCI=3.0V	-	-	7.8	9	mW
Deep sleep mode	PSTPY	VCI=3.0V	-	-	0.003	-	mW
Typical operating current	Iopr_VCI	VCI=3.0V	-	-	2.6	3	mA
Image update time	-	25 °C	-	-	3	5	sec
Sleep mode current	Islp_VCI	DC/DC off No clock No input load Ram data retain	-	-	20		uA
Deep sleep mode current	Idslp_VCI	DC/DC off No clock No input load Ram data not retain	-	-	1	5	uA

Notes: 1. The typical power is measured with following transition from horizontal 2 scale pattern to vertical 2 scale pattern.



- The deep sleep power is the consumed power when the panel controller is in deep sleep mode.
- The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by DKE.

6.3 Panel DC Characteristics(Driver IC Internal Regulators)

The following specifications apply for: VSS=0V, VCI=3.0V, TOPR =25°C.

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
VCOM output voltage	VCOM	-	VCOM	-2.5	-2	-1.5	V
Positive Source output voltage	V _{SH}	-	S ₀ ~S ₁₂₁	+14.5	+15	+15.5	V
Negative Source output voltage	V _{SL}	-	S ₀ ~S ₁₂₁	-15.5	-15	-14.5	V
Positive gate output voltage	V _{gh}	-	G ₀ ~G ₂₄₉	+21	+22	+23	V
Negative gate output voltage	V _{gl}	-	G ₀ ~G ₂₄₉	-21	-20	-19	V

6.4 Panel AC Characteristics

6.4.1 MCU Interface Selection

The pin assignment at different interface mode is summarized in Table 6-4-1. Different MCU mode can be set by hardware selection on BS1 pins. The display panel only supports 4-wire SPI or 3-wire SPI interface mode.

Pin Name	Data/Command Interface		Control Signal		
	D1	D0	CS#	D/C#	RES#
Bus interface	D1	D0	CS#	D/C#	RES#
BS1=L 4-wire SPI	SDIN	SCLK	CS#	D/C#	RES#
BS1=H 3-wire SPI	SDIN	SCLK	CS#	L	RES#

Note: L is connected to V_{ss} H is connected to V_{CI}

6.4.2 MCU Serial Interface (4-wire SPI)

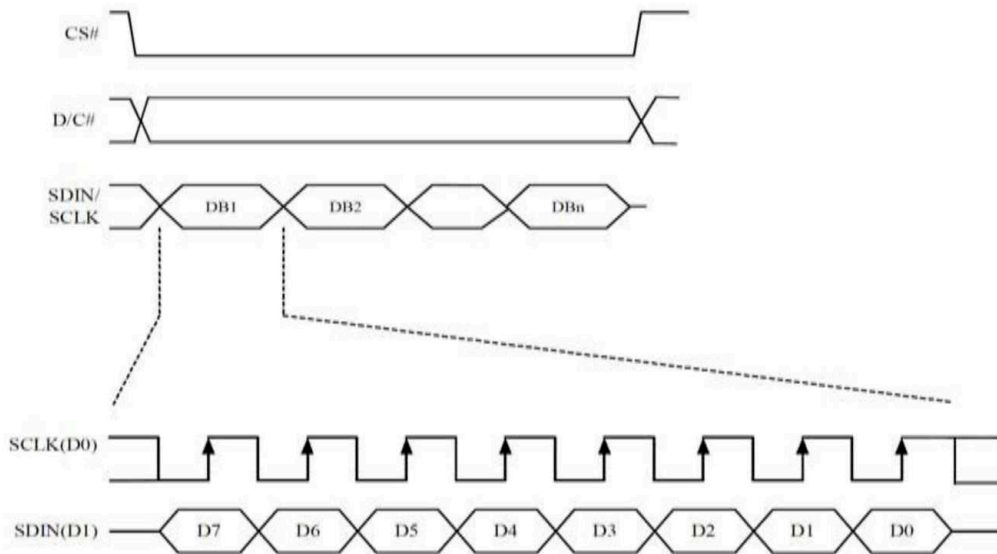
The serial interface consists of serial clock SCL, serial data SDA, D/C#, CS#. This interface supports Write mode and Read mode.

Function	CS#	D/C#	SCL
Write command	L	L	↑
Write data	L	H	↑

Note: ↑ stands for rising edge of signal

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6, ... D0. D/C# is sampled on every eighth clock and the data byte in the shift register is written to the Graphic Display Data RAM (RAM) or command register in the same clock. Under serial mode, only write operations are allowed.

Figure 6-1: Write procedure in 4-wire SPI mode



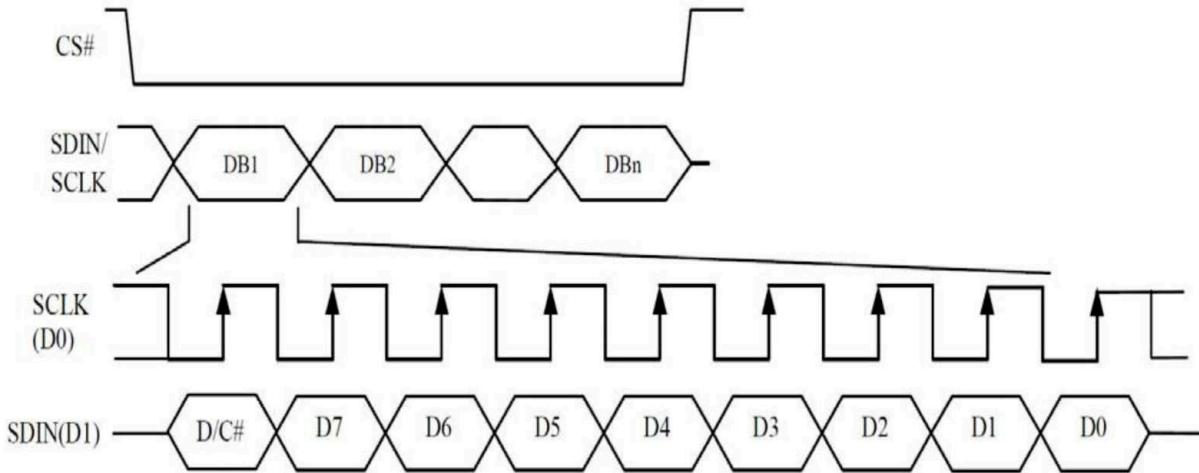
6.4.3 MCU Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCL, serial data SDA and CS#. This interface also supports Write mode and Read mode.

The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0).

Function	CS#	D/C#	SCL
Write command	L	Tie	↑
Write data	L	Tie	↑

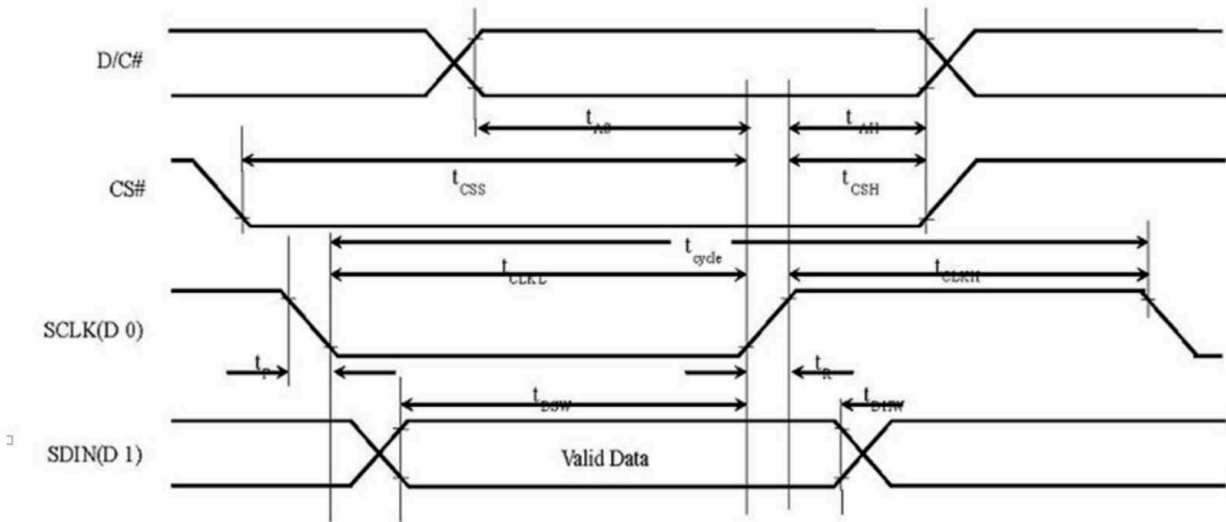
Figure 6-2: Write procedure in 3-wire SPI mode

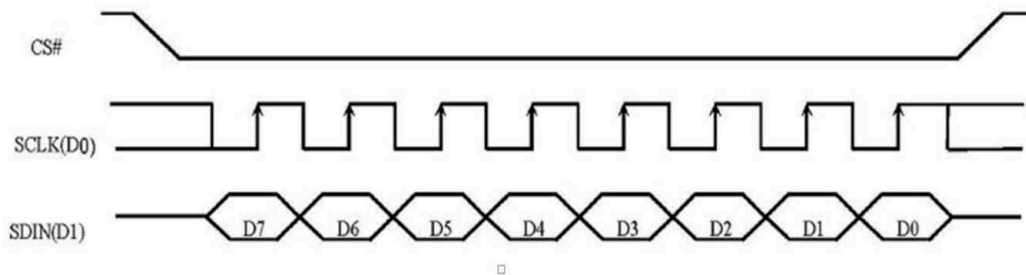


6.4.4 Interface Timing

The following specifications apply for: VSS=0V, VCI=3.0V, T_{OPR} =25°C.

Symbol	Parameter	Test Condition	Applicable pin	Min.	Typ.	Max.	Unit
Fosc	Internal Oscillator frequency	VCI=2.4 to 3.3V	CL	0.95	1	1.05	MHz





Serial Interface Timing Characteristics

(VCI - VSS = 2.2V to 3.7V, TOPR = 25°C, CL=20pF)

Symbol	Parameter	Min	Typ	Max	Unit
Tcycle	Clock Cycle Time	250	-	-	ns
Tas	Address Setup Time	150	-	-	ns
Tah	Address Hold Time	150	-	-	ns
Tess	Chip Select Setup Time	120	-	-	ns
Tesh	Chip Select Hold Time	60	-	-	ns
Tdsw	Write Data Setup Time	50	-	-	ns
Tdhw	Write Data Hold Time	15	-	-	ns
TclkL	Clock Low Time	100			ns
TclkH	Clock High Time	100			ns
Tr	Rise Time [20% ~ 80%]			15	ns
Tf	Fall Time [20% ~ 80%]			15	

7. Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description		
0	0	01	0	0	0	0	0	0	0	1	Driver Output control	Gate setting Set A[7:0]=F9h Set B[7:0]=01h		
0	1		A7	A6	A5	A4	A3	A2	A1	A0				
0	1		0	0	0	0	0	B2	B1	B0				
0	0	03	0	0	0	0	0	0	1	1	Gate Driving voltage control	Set Gate Driving voltage A[4:0]=10h[POR],VGH at 22V[POR] VGH setting from 15V to 22V B[3:0]=0Ah[POR],VGL at 20V[POR] VGL setting from -15V to -20V		
0	1		0	0	0	A4	A3	A2	A1	A0				
0	1		0	0	0	0	B3	B2	B1	B0				
0	0	04	0	0	0	0	0	1	0	0	Source Driving voltage control	SetSource Driving voltage A[7:0]=19h[POR],VSH/VSL at +/- 15V		
0	1		A7	A6	A5	A4	A3	A2	A1	A0				
0	0	10	0	0	0	1	0	0	0	0	Deep Sleep mode	Deep Sleep mode Control		
													A[0] :	Description
0	1		0	0	0	0	0	0	0	A ₀			0	Normal Mode [POR]
											1	Enter Deep Sleep Mode		
0	0	11	0	0	0	1	0	0	0	1	Data Entry mode setting	Define data entry sequence A [1:0] = ID[1:0]Address automatic increment / decrement setting The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. 00 –Y decrement, X decrement, 01 –Y decrement, X increment, 10 –Y increment, X decrement, 11 –Y increment, X increment [POR] A[2] = AM Set the direction in which the address counter is updated automatically after data are written to the RAM. AM= 0, the address counter is updated in the X direction. [POR] AM = 1, the address counter is updated in the Y direction.		
0	1		0	0	0	0	0	A ₂	A ₁	A ₀				
0	0	12	0	0	0	1	0	0	1	0	SWRESET	It resets the commands and parameters to their S/W Reset default values except R10h-Deep Sleep Mode Note: RAM are unaffected by this command.		
0	0	1A	0	0	0	1	1	0	1	0	Temperature Sensor Control	Write to temperature register. A[7:0] – MSByte 01111111[POR] B[7:0] – LSByte 11110000[POR]		
0	1		A7	A6	A5	A4	A3	A2	A1	A0				
0	1		B7	B6	B5	B4	0	0	0	0				

0	0	20	0	0	1	0	0	0	0	0	Master Activation	Activate Display Update Sequence The Display Update Sequence Option is located at R22h User should not interrupt this operation to avoid corruption of panel images.		
0	0	21	0	0	1	0	0	0	0	1	Display Update Control 1	Option for Display Update Bypass Option used for Pattern Display, which is used for display the RAM content into the DisplayOld RAM Bypass option A[7] = 1: Enable bypass A[7] = 0: Disable bypass [POR] A[4] = 0 [POR] A[1:0] Initial Update Option - Source Control		
0	1		0	0	0	0	A3	A2	A1	A0			A[1:0] 01[POR]	GSA GS0
0	0	22	0	0	1	0	0	0	1	0	Display Update Control 2	Display Update Sequence Option: Enable the stage for Master Activation		
												Setting for LUT from MCU		
												Enable Clock Signal, Then Enable Analog Then PATTERN DISPLAY C7 Then Disable Analog Then Disable OSC		
	1		A7	A6	A5	A4	A3	A2	A1	A0		Setting for LUT from OTP according to external Temperature Sensor operation		
											Then Enable Analog Then Load LUT	90		
											Enable Analog Then PATTERN DISPLAY Then Disable Analog Then Disable OSC	47		
0	0	24	0	0	1	0	0	1	0	0	WriteRAM1	After this command, data entries will be written into the 1RAM until another command is written. Address pointers will advance accordingly. For Write pixel: Content of write RAM(BW)=1 For Black pixel: Content of write RAM(BW)=0		
0	0	2C	0	0	1	0	1	1	0	0	Write VCOM register	Set A[7:0]=7Bh		
0	1		A7	A6	A5	A4	A3	A2	A1	A0	VCOM Register Read	Read VCOM Register: 1. A[7:0]=00H 2. B[7:0]: VCOM Register		
0	0	2D	0	0	1	0	1	1	0	1				
1	1		A7	A6	A5	A4	A3	A2	A1	A0				
1	1		B7	B6	B5	B4	B3	B2	B1	B0				
0	0	2F	0	0	1	0	1	1	1	1	Status Bit Read	Read IC status Bit A[1:0]: chip ID [POR=01] A[2] : Busy flog [POR=0]		
1	1		0	0	0	0	0	A2	A1	A0				

8. Optical Specification

Measurements are made with that the illumination is under an angle of 45 degree, the detection is perpendicular unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ.	Max	Units	Notes
R	White Reflectivity	White	30	35	-	%	8-1
CR	Contrast Ratio	indoor	8:1		-		8-2
Gn	2Grey Level	-	-	$DS+(WS-DS)*n(m-1)$			8-3
T update	Image update time	at 25 °C	-	3	-	sec	
Life		0°C~50°C		1000000times or 5years			

Notes: 8-1 Luminance meter: Eye-One Pro Spectrophotometer.

8-2 CR=Surface Reflectance with all white pixel/Surface Reflectance with all black pixels.

8-3 WS: White state, DS: Dark state

9. Handling, Safety, and Environment Requirements

Warning

The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

Caution

The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components. Disassembling the display module.

Disassembling the display module can cause permanent damage and invalidates the warranty agreements.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

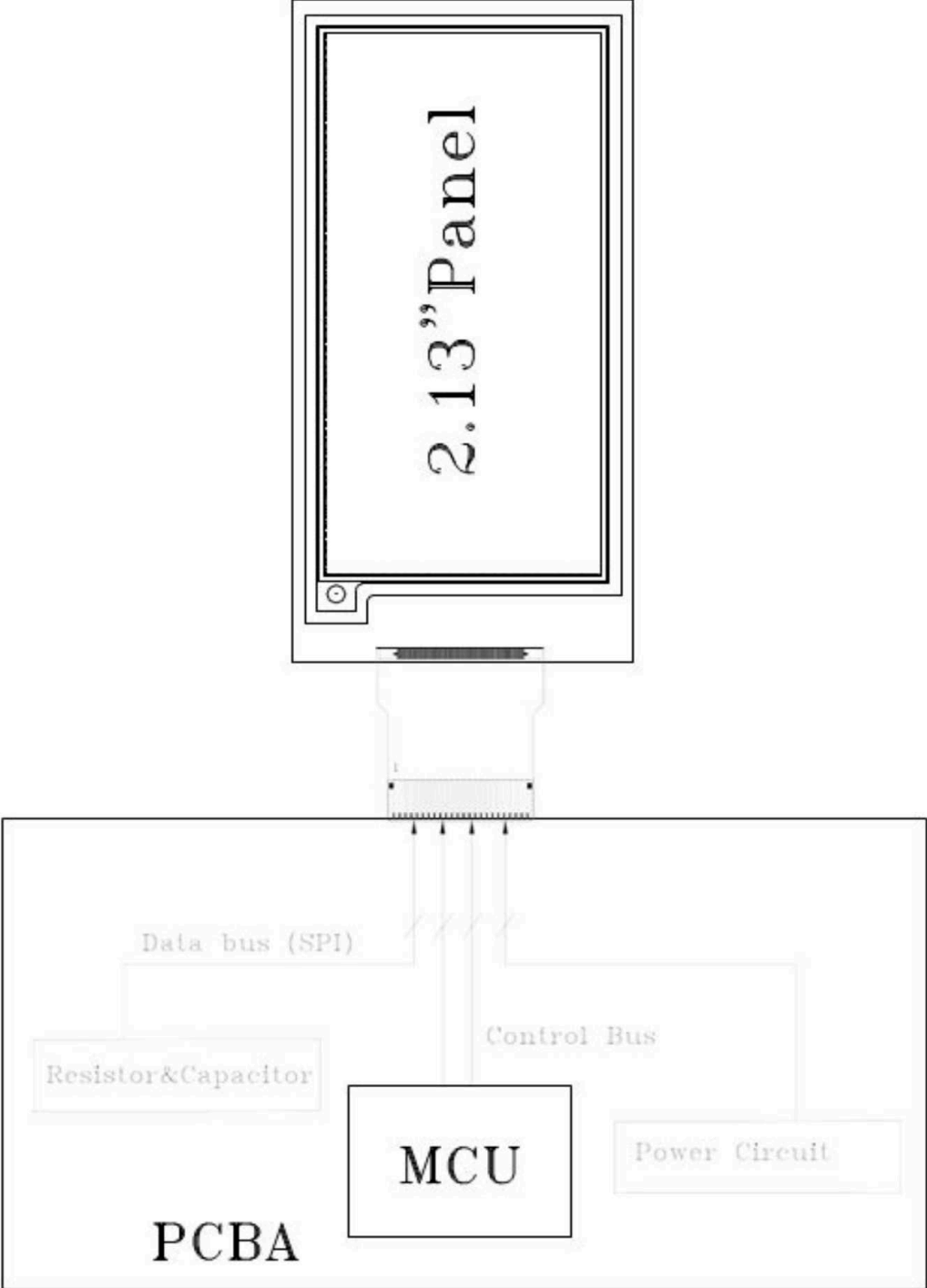
Data sheet status	
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

10. Reliability Test

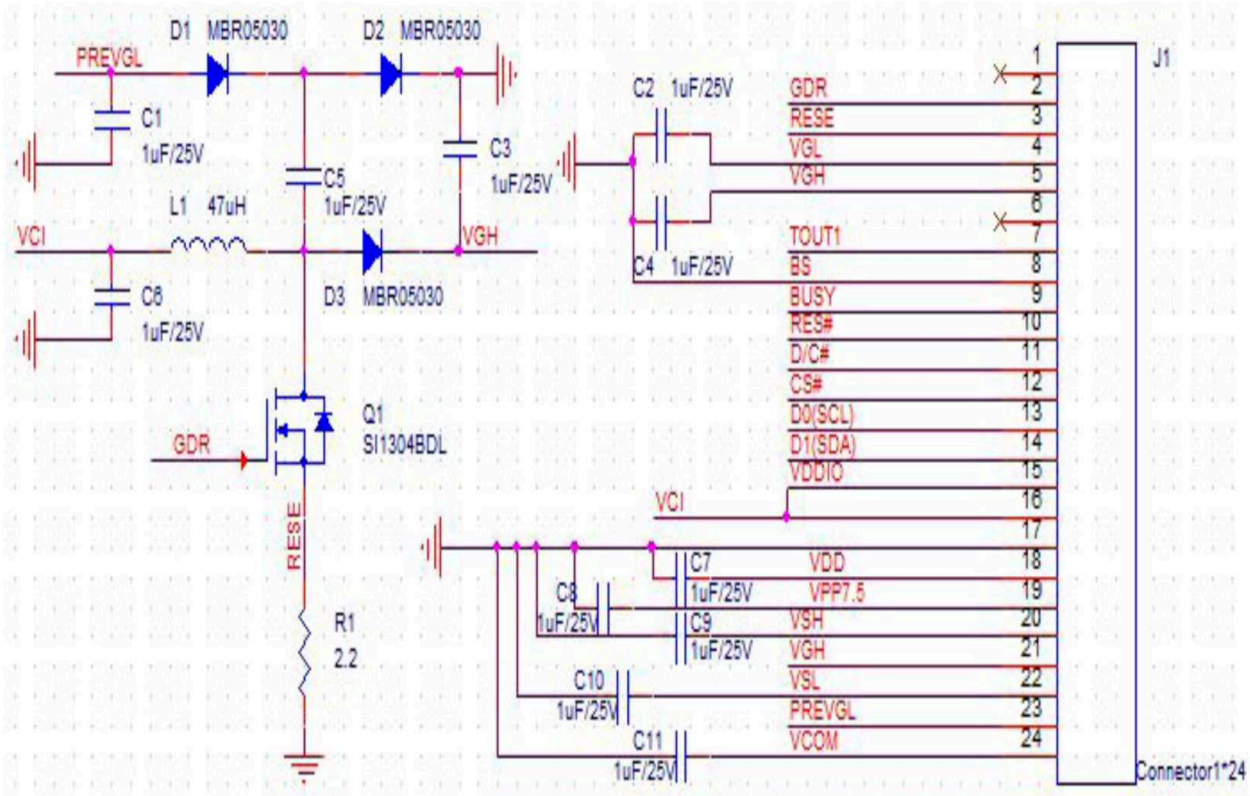
NO	Test items	Test condition
1	Low-Temperature Storage	T = -25°C, 240 h Test in white pattern
2	High-Temperature Storage	T = +70°C, RH=40% ,240h T=+60°C, RH=26%,240h Test in white pattern
3	High-Temperature Operation	T = +50°C, RH = 30% ,240h
4	Low-Temperature Operation	0°C, 240h
5	High-Temperature, High-Humidity Operation	T=+40°C, RH=90%,168h
6	High Temperature, High Humidity Storage	T=+60°C, RH=80%,240h Test in white pattern
7	Temperature Cycle	1 cycle:[-25°C 30min]→[+70 °C 30 min] : 100 cycles Test in white pattern
8	UV exposure Resistance	765W/m ² for 168hrs,40 °C Test in white pattern
9	ESD Gun	Air+/-15KV;Contact+/-8KV (Test finished product shell,not display only) Air+/-8KV;Contact+/-6KV (Naked EPD display,no including IC and FPC area) Air+/-4KV;Contact+/-2KV (Naked EPD display,including IC and FPC area)

Note: Put in normal temperature for 1hour after test finished, display performance is ok.

11. Block Diagram



12. Typical Application Circuit with SPI Interface



13 . Typical Operating Sequence

13.1 Normal Operation Reference Program Code

ACTION	VALUE/DATA	COMMENT
POWER ON		
delay	10ms	
PIN CONFIG		
RESE#	high	Hardware reset
delay	200us	
RESE#	low	
delay	200us	
Read busy pin		Wait for busy low
Command 0x12		Software reset
Read busy pin		Wait for busy low
Command 0x01	Data 0xf9 0x01	Set display size and driver output control
Command 0x11	Data 0x03	Ram data entry mode
Command 0x44	Data 0x00 0x0F	Set Ram X address
Command 0x45	Data 0x00 0XF9	Set Ram Y address
Command 0x3C	Data 0x01	Set border
SET VOLTAGE AND LOAD LUT		
Command 0x2C	Data 0x7B	Set VCOM value
Command 0x03	Data 0x100x0A	Gate voltage setting
Command 0x04	Data 0x19	Source voltage setting
Command 0x3A	Data 0x06	Frame setting 50hz
Command 0x3B	Data 0x0B	
Command 0x32	Write 29bytes LUT	Load LUT
LOAD IMAGE AND UPDATE		
Command 0x4E	Data 0x00	Set Ram X address counter
Command 0x4F	Data 0x00	Set Ram Y address counter
Command 0x24	4000bytes	Load image (128/8*250)
Command 0x22	Data 0XC7	Image update
Command 0x20		
Read busy pin		Wait for busy low
Command 0x10	Data 0X01	Enter deep sleep mode
POWER OFF		
ACTION	VALUE/DATA	COMMENT
POWER ON		
delay	10ms	
PIN CONFIG		
RESE#	high	Hardware reset

13.2 Partial update Operation Reference Program Code

ACTION	VALUE/DATA	COMMENT
POWER ON		
delay	10ms	
PIN CONFIG		
RESE#	high	Hardware reset
delay	200us	
RESE#	low	
delay	200us	
Read busy pin	Wait for busy low	
Command 0x12		Software reset
Read busy pin	Wait for busy low	
Command 0x01	Data 0xf9 0x01	Set display size and driver output control
Command 0x11	Data 0x03	Ram data entry mode
Command 0x44	Data 0x00 0x0F	Set Ram X address
Command 0x45	Data 0x00 0XF9	Set Ram Y address
Command 0x3C	Data 0x01	Set border
SET VOLTAGE AND LOAD LUT		
Command 0x2C	Data 0x7B	Set VCOM value
Command 0x03	Data 0x100x0A	Gate voltage setting
Command 0x04	Data 0x19	Source voltage setting
Command 0x3A	Data 0x06	Frame setting 50hz
Command 0x3B	Data 0x0B	
Command 0x32	Write 29bytes LUT	Load LUT
LOAD IMAGE AND FULL UPDATE		
Command 0x4E	Data 0x00	Set Ram X address counter
Command 0x4F	Data 0x00	Set Ram Y address counter
Command 0x24	4000bytes	Load image (128/8*296)
Command 0x22	Data 0XC7	Image update
Command 0x20		
Read busy pin	Wait for busy low	
Command 0x4E	Data 0x00	Set Ram X address counter
Command 0x4F	Data 0x00	Set Ram Y address counter
Command 0x24	4000bytes	Load image (128/8*296)
Command 0x22	Data 0XC7	Image update
Command 0x20		
Read busy pin	Wait for busy low	
LOAD PARTIAL UPDATE LUT AND ANALOG ON		
Command 0x32	Write 29bytes Partial LUT	Load Partial LUT
Command 0x22	Data 0XC0	Analog on
Command 0x20		
Read busy pin	Wait for busy low	
PARTIAL UPDATE SEQUENTIAL PICTURES		
Command 0x44	Data 0xXX 0xXX	Set partial update Ram of picture1
Command 0x45	Data 0xXX 0xXX 0xXX0xXX	
Command 0x4E	Data 0xXX	
Command 0x4F	Data 0xXX 0xXX	
Command 0x24	N bytes	Load partial picture1datas
Command 0x22	Data 0X04	Partial update
Command 0x20		
Read busy pin	Wait for busy low	

Read busy pin	Wait for busy low	
Command 0x44	Data 0xXX 0xXX	Set partial update Ram of picture2
Command 0x45	Data 0xXX 0xXX 0xXX0xXX	
Command 0x4E	Data 0xXX	
Command 0x4F	Data 0xXX 0xXX	
Command 0x24	N bytes	Load partial picture2 data
Command 0x22	Data 0X0C	partial update
Command 0x20		
Read busy pin	Wait for busy low	
:	:	:
:	:	:
Command 0x44	Data 0xXX 0xXX	Set partial update Ram of picture N
Command 0x45	Data 0xXX 0xXX 0xXX0xXX	
Command 0x4E	Data 0xXX	
Command 0x4F	Data 0xXX 0xXX	
Command 0x24	N bytes	Load partial picture N data
Command 0x22	Data 0X0C	partial update
Command 0x20		
Read busy pin	Wait for busy low	
ANALOG OFF		
Command 0x22	Data 0X03	Analog off
Command 0x20		
Read busy pin	Wait for busy low	
Command 0x10	Data 0X01	Enter deep sleep mode
POWER OFF		

Note: During partial update the IC should not enter deep sleep mode.

14. Inspection condition

14.1 Environment

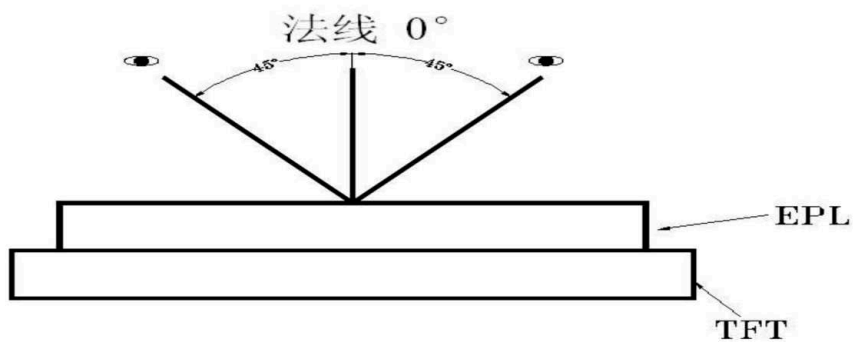
Temperature: $25\pm 3^{\circ}\text{C}$

Humidity: $55\pm 10\%\text{RH}$

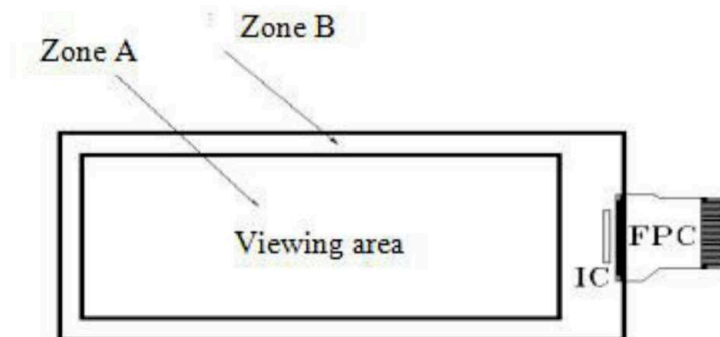
14.2 Illuminance

Brightness: $1200\sim 1500\text{LUX}$; distance: $20\text{-}30\text{CM}$; Angle: Relate 30° surround.

14.3 Inspect method

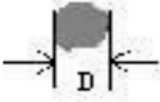
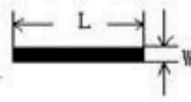


14.4 Display area

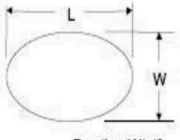
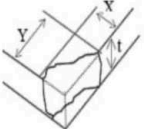



14.5 Inspection standard

14.5.1 Electric inspection standard

NO.	Item	Standard	Defect level	Method	Scope
1	Display	Display complete Display uniform	MA	Visual inspection	
2	Black/White spots	 $D \leq 0.25\text{mm}$, Allowed $0.25\text{mm} < D \leq 0.4\text{mm}$, $N \leq 3$, and Distance $\geq 5\text{mm}$ $0.4\text{mm} < D$ Not Allow	MI		
3	Black/White spots (No switch)	 $L \leq 0.6\text{mm}$, $W \leq 0.2\text{mm}$, $N \leq 1$ $L \leq 2.0\text{mm}$, $W > 0.2\text{mm}$, Not Allow $L > 0.6\text{mm}$, Not Allow		Visual/ Inspection card	Zone A
4	Ghost image	Allowed in switching process	MI	Visual inspection	
5	Flash spots/ Larger FPL size	Flash spots in switching, Allowed FPL size larger than viewing area, Allowed	MI	Visual/ Inspection card	Zone A Zone B
6	Display wrong/Missing	All appointed displays are showed correct	MA	Visual inspection	Zone A
7	Short circuit/ Circuit break/ Display abnormal	Not Allow			

14.5.2. Appearance inspection standard

NO.	Item	Standard	Defect level	Method	Scope
1	B/W spots /Bubble/ Foreign bodies/ Dents	 <p>$D = (L + W) / 2$</p> <p>$D \leq 0.25\text{mm}$, Allowed $0.25\text{mm} < D \leq 0.4\text{mm}$, $N \leq 3$ $D > 0.4\text{mm}$, Not Allow</p>	MI	Visual inspection	Zone A
2	Glass crack	Not Allow	MA	Visual / Microscope	Zone A Zone B
3	Dirty	Allowed if can be removed	MI		Zone A Zone B
4	Chips/Scratch/ Edge crown	<p>$X \leq 3\text{mm}, Y \leq 0.5\text{mm}$</p>  <p>$2\text{mm} \leq X$ or $2\text{mm} \leq Y$ Allow</p> <p>$W \leq 0.1\text{mm}, L \leq 5\text{mm}, n \leq 2$ Edge crown: $X \leq 0.3\text{mm}, Y \leq 3\text{mm}$</p>	MI	Visual / Microscope	Zone A Zone B
5	Substrate color difference	Allowed			
6	FPC broken/ Goldfingers oxidation/ scratch	 <p>Not Allow</p>	MA	Visual / Microscope	Zone B

7	PCB damaged/ Poor welding/ Curl	PCB (Circuit area) damaged Not Allow PCB Poor welding Not Allow PCB Curl \leq 1%	MI	Visual / Ruler	Zone B
8	Edge Adhesives height/FPL/ Edge adhesives bubble	Edge Adhesives height \leq Display surface Edge adhesives seep in \leq 1/2 Margin width FPL tolerance \pm 0.3mm Edge adhesives bubble: bubble Width \leq 1/2 Margin width; Length \leq 0.5mm。 n \leq 3			
9	Protect film	Surface scratch but not effect protect function, Allow			